AN17

Wideband, Low Distortion Techniques

WIDEBAND, LOW DISTORTION TECHNIQUES FOR MOSFET POWER AMPS

Shake table systems, function generators and acoustic instruments all have requirements similar to quality audio amplifiers: wide bandwidths along with low distortion. In the past, industrial grade power op amps have traded off bandwidth to insure unity gain stability, and the bipolar designs have not always met the linearity requirements of demanding applications. The PA04 changes all this with a MOSFET based architecture that sets new standards for bandwidth and linearity of integrated circuit power amplifiers.

The development of the PA04 was driven by sonar application requirements for a highly linear, high power amplifier with a power bandwidth in excess of 100 kHz. MOSFET's are the optimum choice power device to provide this performance, and in the PA04 Apex Microtechnology goes several steps further in using MOSFET's in all active gain stages. While this application note will focus on getting best bandwidth and linearity from the PA04, the techniques described apply to any power op amp.

Op amps depend on negative feedback to improve performance in all ways including accuracy, linearity and bandwidth. The ideal condition is to use feedback around a design which has inherently good open loop characteristics. Evaluation of prospective amplifiers under open loop conditions quickly reveals linearity and bandwidth deficiencies. Even a simple distortion measurement under open loop conditions will give rapid comparative evaluation. Alternatively, an X-Y comparison using an oscilloscope and the circuit of Figure1, which multiplies summing node error by 100, will give a visual display of amplifier linearity. The circuit of Figure 1 will reveal that PA04 has an inherently linear characteristic while even the best bipolar designs such as PA07 have quite a bit of curvature in their open loop linearity. This is traceable to the better inherent linearity of MOSFET devices in comparison to bipolar transistors.

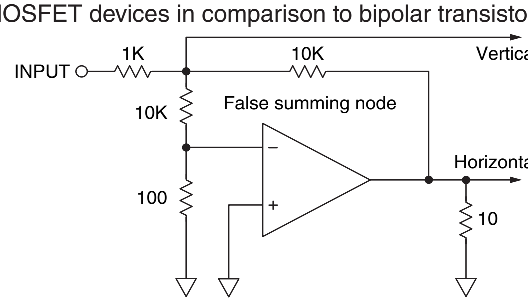

FIGURE 1. SIMPLE TEST CIRCUIT

CIRCUIT CONSIDERATIONS

The design considerations desirable for wideband, low distortion designs can be summed up with four guidelines:

1. Lowest possible closed loop gain.
2. Inverting configuration.
3. External phase compensation.
4. Input slew-rate limiting.

Distortion reduction in an op amp circuit is proportional to the amount of feedback, and this corresponds to lower gain circuits having reduced distortion. Distortion reduction is described mathematically as:

$$Df = D\left(\frac{Af}{A}\right)$$

Where: Df = % DISTORTION WITH FEEDBACK
D = % DISTORTION OPEN LOOP
A = OPEN LOOP GAIN
Af = CLOSED LOOP GAIN

It is obvious that open loop distortion is an important criteria in amplifier selection. A high open loop gain is also desirable, but op amps with high open loop gains most often have a severe tradeoff in gain-bandwidth.

The minimum useful closed loop gain is determined by the amplitude of the drive signal available to the power op amp circuit. Most often this drive is likely to come from a small signal op amp with the customary ±10 V peak drive capability. If for example a PA04 power op amp is being designed which operates at the full ±100 V supply rail limit of the PA04, this will require a minimum gain of 10.

In the event the drive signal is not a full ±10V peak, a tradeoff must be made as to whether the power op amp should be operated at a higher gain, or an additional small signal op amp be included for additional gain. Consider that the additional small signal op amp will result in insignificant contributions to distortion as long as its gain is low (<30). The light loading of the power amp circuit further minimizes distortion from the small signal op amp. These considerations favor this multiple op amp approach with a lower gain power op amp compared to a single high gain power op amp.

Low closed loop gain in the power op amp equates to increased amounts of negative feedback. This condition occasionally meets with unfounded objections when the requirement is low distortion, especially under transient conditions. However, this is dealt with by slew rate limiting to be discussed later.

The inverting amplifier configuration forces common mode potentials to zero. By doing so, non-linearities due to common-mode effects are also reduced to zero. The main advantage a non-inverting configuration would have is greater freedom of design regarding input impedance of the power op amp circuit along with the obvious lack of inversion.

Although the inverting configuration reduces input impedance, the two amplifier approach insures that the power amp circuit is driven by a source adequate to handle the resultant impedance. The cascade of two inverting amplifiers yields a non-inverting circuit. A further possible useful feature of the inverting power amp circuit is that the summing node can be monitored and any voltage detected used to indicate fault or non-linear conditions.

EXTERNAL PHASE COMPENSATION

Many power op amps are internally compensated for unity gain stability. However, this trades off gain-bandwidth product for stability under all operating conditions. Since distortion reduction is proportional to the ratio of open loop to closed loop gain, it is desirable to have as high as possible open-loop gain at high frequencies. Since it is unlikely that the power op amp will be configured for unity gain, the external phase compensation allows for a reduced compensation, yielding improved distortion and slew performance.

The small signal response curve for PA04 shown in Figure 2 helps to illustrate the comparative advantage of external phase compensation. The straight line at 20dB represents a gain of 10 amplifier which if the PA04 were compensated for unity gain would provide a 200 kHz rolloff. Decompensation for a gain of 10 results in a 700 kHz rolloff. In addition, note that loop gain for the unity-gain compensation is only 22 dB at 20 kHz, while it is 30 dB for the gain of 10 compensation. This increase in loop gain results in 2.5 times less distortion at 20 kHz.

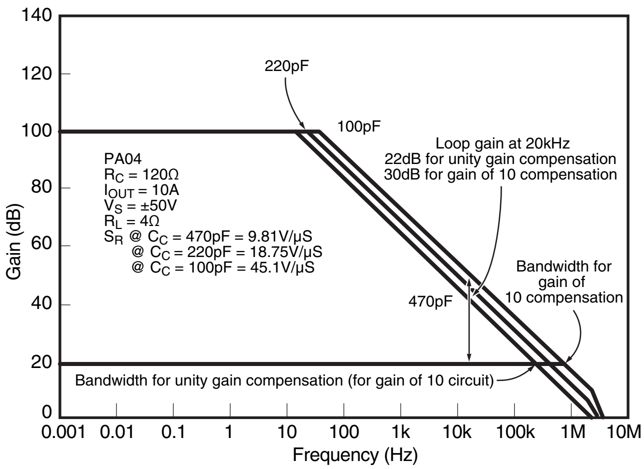

FIGURE 2. THE SMALL SIGNAL RESPONSE FOR THE PA04

The large amount of feedback at low gains obviously reduces distortion. Problems can occur however under transient conditions. If a step function is applied to the input of the amplifier circuit, the output can only change as fast as the amplifier slew rate allows. During this slew interval the input summing node will develop a large differential voltage. This nonlinear condition and input overload can cause a host of difficulties including a slow and poorly behaved recovery from this overload.

Restriction of the input slew rate can avoid these transient distortion problems. The input should never be allowed to slew faster than the amplifier output can follow. If the actual slew rate of the source cannot be predicted or controlled, then simple low pass filtering at the amplifier input will prevent transient distortion.

The filter time constant is a function of amplifier slew rate. The maximum acceptable rate-of-change on the input signal is limited to a value less than the amplifier slew rate divided by the amplifier gain. With a known maximum step function input, the maximum rate-of-change at the low pass filters output occurs at t=0 and is determined by:

$dv/dt = (V/R)/C$

The RC time constant trc required at the amplifier input is:

$trc = (V_{IN}A_V)/S_R$

Where: V_{IN} = PEAK-TO-PEAK INPUT VOLTAGE
A_V = CLOSED LOOP GAIN
S_R = SPECIFIED AMPLIFIER SLEW RATE

Note that there is some reduction in bandwidth with this filter. However, with the PA04 this still permits a 40 kHz bandwidth. This limitation again favors the use of the fastest possible power amplifiers. Keep in mind that transient behavior is actually enhanced by the addition of the input filter.

STABILITY CONSIDERATIONS

When a power amplifier drives a capacitive load, the interaction between output resistance and capacitive load creates an additional pole and attendant phase shift in amplifier response (Figure 3). Inductive loads can result in stability problems due to rising impedances at high frequencies. Most follower type output stages are immune to the effects of inductive loads, but collector output, drain output and quasi-complementary output stages with local feedback loops are susceptible to parasitic oscillations driving inductive loads.

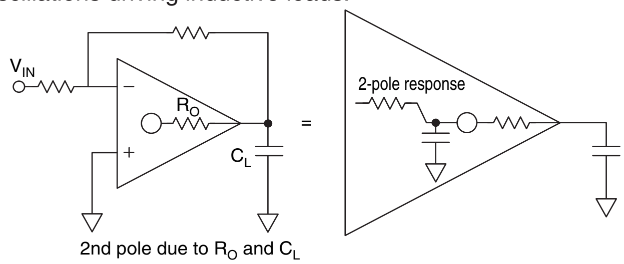

FIGURE 3. CAPACITIVE OP AMP LOADS

Figure 4 shows several measures are available to improve stability, each with some advantage and disadvantage: (a.) Capacitor across feedback resistor. This provides a compensating phase lead in the feedback path to counteract the effects of additional poles. This technique generally requires a unity-gain stable amplifier. (b.) Parallel inductor-resistor combination in

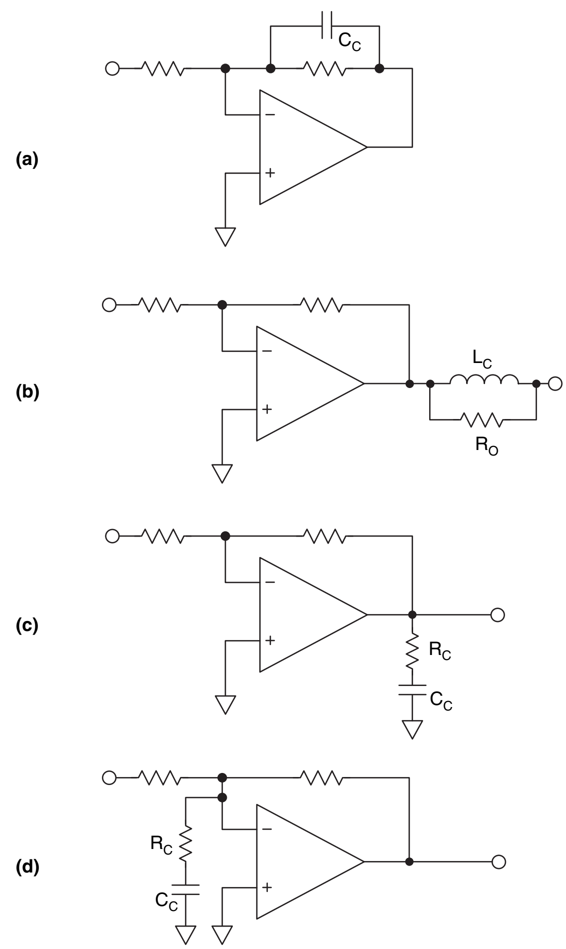

FIGURE 4. STABILITY ENHANCING TECHNIQUES

series with amplifier output. Feedback must be taken directly at output of amplifier so that inductor-resistor has the effect of isolating the amplifier and feedback network from the capacitive load. (c.) Series resistor and capacitor from amplifier output to ground, often referred to as a snubber. Used only in situations where amplifiers are sensitive to inductive loads. Insures a low, resistive load impedance at high frequencies. (d.) Series R-C network across op amp inputs, often referred to as noise-gain compensation. Simply described, this technique reduces feedback at high frequencies to the point where stability is not a problem.

Methods a and b offer the best overall bandwidth performance and transient behavior. Method a has been mentioned already as having the tradeoff of requiring a unity gain stable amplifier. However, with proper attention to design, it is possible to incorporate method a with any amplifier to help control overshoot and ringing behavior.

Method d, the noise gain compensation, will have the effect of reducing the closed loop bandwidth of the resultant circuit to the same effective closed loop bandwidth corresponding to the noise gain. To illustrate, consider a gain of 10 amplifier with a network across the inputs configured for a high frequency noise gain of 100. If the gain of 10 amplifier had an uncompensated bandwidth of 100 kHz, with the noise gain compensation, the bandwidth would be reduced to 10 kHz. In addition, the response curve peaks near the high frequency limit resulting in overshoots in the square wave response.

All amplifiers vary in their ability to tolerate capacitive loading before stability problems occur. PA04 is especially good in this regard tolerating well over 1 uF while operating at a gain of 10. In the case of PA04, no additional stability enhancement measures are required and this is the ideal case for best frequency response.

TYPICAL DESIGN EXAMPLE

A design utilizing all of the guidelines described here would be constructed around a PA04 in an inverting gain of 10 configuration as shown in Figure 5. For additional gain the PA04 is preceded by a small signal op amp also operating at an inverting gain of 10. Many choices are available for this op amp such as the 5534 or OP37. The PA04's tolerance of reactive loads negates the need for additional stability enhancement components.

With an 8 ohm load this circuit can supply over 300W at up to 150 kHz with the input slew rate filter bypassed. With the filter in place, gain begins to rolloff at 40kHz, although full output swing is available up to 150kHz. Distortion never exceeds 0.02% THD. Power supplies will need to be capable of at least 7A to support 8 ohm loads in ac coupled applications. Regulated supplies aren't necessary but are desirable from a reliability standpoint.

When designing for low distortion with PA04, the impedance of the feedback and input networks around the op amp should be kept as low as possible. The input MOSFET's of the PA04 cause it to have a large input capacitance which is nonlinear with variations in input signal. Excessive impedances will increase distortion due to these higher order capacitance effects. The 2K ohm input resistor of Figure 5 is high enough to avoid excessive loading of the small signal op amp and low enough to avoid distortion effects with the PA04.

Several basic practices are important to implement when using PA04. Power supply bypassing consisting of good high frequency capacitors, generally ceramic, must be connected from each supply rail to ground. Unless these capacitors are physically close to the amplifier, parasitic oscillations may occur. Even an inch away from the socket pins is too far. Be sure to read and observe all ESD precautions on the PA04 data sheet, and those shipped with PA04.

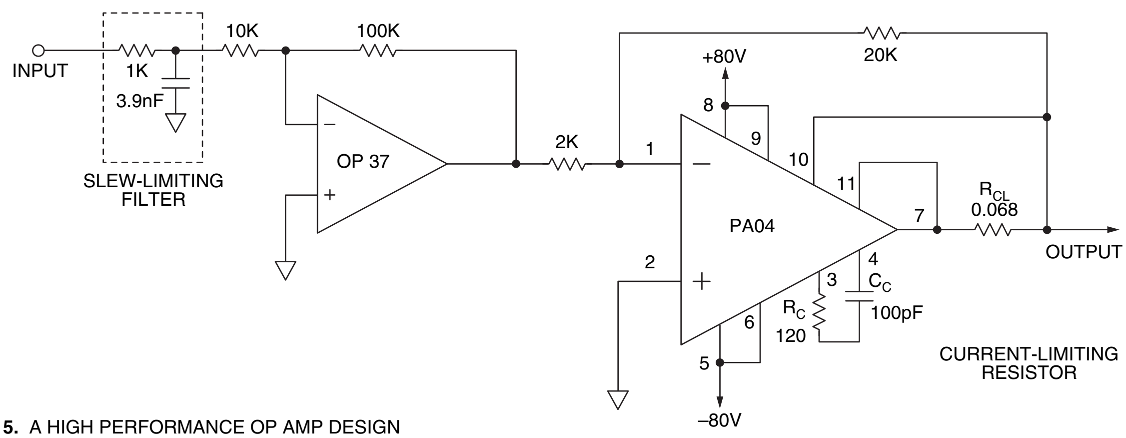

FIGURE 5. A HIGH PERFORMANCE OP AMP DESIGN

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